Remarks

Claims 1-4 and 8-19 are pending in the instant application. Claims 5-7 and 20-26 were withdrawn as being drawn to a non-elected group and species. Claims 1 and 19 have been amended; the amendments have basis in the original specification.

§ 112 Rejections

The Examiner has rejected claim 19 under 35 U.S.C. §112, first paragraph, as not being enabled. Specifically, the Examiner has stated that claim 19 should be dependent upon claim 18 rather than claim 1. Upon review it appears the Examiner is correct, and claim 19 has been so amended. Applicants therefore respectfully request that the rejection under 35 U.S.C. §112, second paragraph, be withdrawn.

§ 102 Rejections

The Examiner has rejected claim 1 under 35 U.S.C. §102 as being anticipated by Higgins. Applicants respectfully traverse the rejection. Applicants dispute this fact for the following reasons. Higgins discloses the concept of EMI shielding of the chip package by the application of external layers of insulating, inductive and/or conducting material. The Applicants contend that Higgins does not disclose and will not generate meaningful capacitance in the IC substrate.

In his argument the Examiner points specifically to figure 3 as grounds on which to base the rejection. Figure 3 refers to a particular construction of an electronic component assembly (10) with multiple over-layers (24, 60, 62, and 64). Higgins refers to the supporting substrate (16) as a conventional printed wiring board (PWB) or interconnect substrate (column 5 lines 42 to 46).

The Examiner states that Higgins discloses in figure 3, a capacitor including a first conductive layer (22), a second conductive layer (25) and a dielectric material disposed between these conductive layers such that the first conductive layer is mounted adjacent to the second side of the conductive traces (18). In the specification, Higgins describes feature 25 as a power plane and feature 27 as an EMI ground plane. While not certain of its engineering feasibility, for the sake of addressing the Examiner's concerns, the Applicants acknowledge that it may be possible to exchange the functional purpose of these planes such that the ground plane could be located at the location of feature 25 in the drawing. We will refer to this modified plane as ground plane 25'. Feature 22 is a transverse circuit trace (column 5, line 55) and given the conventional understanding of the terminology is probably

not a continuous plane of copper, but rather a thin copper strip that has small area. Any capacitance inherent in the system (consisting of 22 and the ground plane 25') is therefore very small and is incidental (and not intentionally derived) by the geometry of the system.

Closer examination of the Figure 3 reveals that feature 25 is a power plane that would generate some capacitance by virtue of the geometry with feature 27, the EMI ground plane. As before, such capacitance would be very small and incidental (and not intentionally derived) by the geometry of the system.

The equation: $\left(C/A\right)=\frac{\varepsilon_0 k}{t}$ (where ε_0 is the permittivity of free space, k is the dielectric constant of the insulating material, t is the insulator thickness, and C/A is the capacitance per unit area) can be used to calculate the available capacitance of a parallel plate capacitor. This equation reduces to the approximation:

$\left(C/A\right)=\frac{0.885\times k}{t}$ where C/A is in nanoFarrads/cm^2 (nF/cm^2) and t is in microns.

Given the typical values of thickness and dielectric constant of FR-4 (a typical PWB insulating dielectric material) of 160 microns and 4 respectively, the C/A of this layer is about 24 picoFarads/cm^2 — too small to provide a measurable effect on IC performance.

Higgins discloses conductive traces or pads (18). Feature 21 does not refer to a conductive trace as the Examiner asserts but rather to a power ground plane. The dielectric substrate (24) that the Examiner cites as being mounted on the first side of the conductive traces is an insulating conformal coating (1-250 μm thick) for encapsulating the die and substrates to prevent electrical shorts. The Examiner appears to indicate that this external layer (24) may be used as a capacitor dielectric by capacitively coupling planes within the interconnect substrate. Higgins describes layer 24 as a polymer coating loaded with ceramic particles (column 6, lines 20-35) and given the application techniques (coating) it may be possible to obtain a dielectric constant of 20 in this layer. The capacitance generated from this layer, if any, will be very limited by the area (limited by a layer thickness and length of the layer (several cm). The C/A may be of the order of 1 pF/cm^2 over a very limited area. However, nowhere does Higgins teach that this layer offers any capacitive benefit.

In view of these facts, Applicants believe that no capacitor was provided as this layer does not offer meaningful capacitance. Applicants have amended claim 1 to clarify that the capacitor built into the electronic package claimed by Applicants provides capacitance to the package. Applicants respectfully request that the Examiner withdraw the rejection under 35 U.S.C. §102 over Higgins.

The Examiner has also rejected claims 1-3, 12 and 17 under 35 U.S.C. §102 as being anticipated by Kabumoto. Applicants also respectfully traverse this rejection. This patent is concerned with a particular construction of ceramic package incorporating a power and ground plane. Although Kabumoto acknowledges the benefit of having capacitance (column 2, lines 14-18) within the package, he envisages a multi-layer capacitor (column 2, lines 21-32) which he discounts as being too bulky with the available dielectric constant of the substrate (column 2, lines 42-49). The patent then focuses on using these closely spaced planes as a low inductance path to the IC from an externally mounted chip capacitor (feature 9 in Figure 1). Kabumoto does not teach and will not produce significant capacitance from this internal plane structure. The use of an external chip decoupling (column 5, lines 23-34) capacitor (typical value may be ~100 nanoFarrads) is acknowledgement of this fact.

The Examiner points out the existence of a capacitor between layers 10 and 11 in figure 1. Kabumoto does not "disclose" this as a capacitor but rather a low inductance plane pair. It is true that geometrically a capacitor would be generated although, as illustrated above, the capacitive value is too low to be useful.

Given the geometry described in column 3, lines 24-28 and the dielectric constant of 7 (column 2, line 45), a capacitance per unit area of ~60 picoFarrad/cm^2 may be generated. This is three orders of magnitude less than the typical capacitance of an external chip capacitor, and therefore will provide a negligible improvement in the capacitive performance of the whole package.

Although Kabumoto illustrates the need for layers less than 0.1 mm to generate low inductance planes (column 6, lines 39-47), he does stress the difficulty in generating these thin layers. Given Kabumoto's recited manufacturing process, he proposes (column 4, lines 7-18) that anyone skilled in the art would recognize that the layer thickness must be limited to approximately 50 μm order to be handled. Taking this geometry into account, the capacitance generated would be about 120 pF/cm^2, which is still too small to have a significant effect on IC performance.

With regard to claim 3, the Examiner states that the heatsink (H) is synonymous with Applicants' stiffening member. Kabumoto teaches the use of the heatsink for it original intended purpose. He does not teach using the heatsink (H) as a stiffening member is not required in conjunction with a ceramic package. He also does not specifically teach that the heatsink must be metallic, although at the time that this patent was filed the majority of

heatsinks were metallic although ceramic heatsinks were also available and now with recent advances filled polymeric heatsinks are now available.

With regards to claim 12, the Examiner states that the dielectric material includes a metal oxide. The package described in Kabumoto does indeed utilize sintered aluminum oxide as the dielectric material; the invention described by the Applicants details the use of a dispersed metal oxide in a polymeric binder material. Further, the sintered aluminum oxide material described in Kabumoto does not have the required dielectric constant to be of use in Applicants' invention.

Applicants have amended claim 1 to clarify that the capacitor built into the electronic package claimed by Applicants provides capacitance to the package. Applicants respectfully request that the Examiner withdraw the rejection under 35 U.S.C. §102 over Kabumoto.

§ 103 Rejections

The Examiner has rejected claim 4 under 35 U.S.C §103 as being unpatentable over Kabumoto as previously applied and further in view of Dehaine et al.

Dehaine (US 4,982,311) describes a package for a VSLI chip, which utilizes external decoupling capacitors. Dehaine has no teaching of suggestion of providing significant capacitance from the internal conductive face structure. The use of the external decoupling capacitors is acknowledgement of this fact. The Examiner says that Dehaine teaches the device receiving region extending through the capacitor layer, but since the conductive face structure is not the true capacitor in this package, this is not supported by the disclosure.

The Examiner has further rejected claims 8-10 as being unpatentable over Kabumoto as applied and further in view of Parker et al.

Claims 14-16, 18, and 19 are rejected as being unpatentable over Kabumoto as applied and further in view of Fujisawa et al.

The Examiner has further rejected claims 11 and 13 as being unpatentable over Kabumoto as applied and further in view of Brandt et al.

Applicants submit that the arguments related to Kabumoto discussed above also apply to the obviousness rejection. Kabumoto does not teach or suggest significant capacitance from the internal plane structure disclosed. Applicants respectfully suggest that a reference having a structure which cannot provide meaningful capacitance will not render Applicants' invention obvious to one of skill in the art. As the additional references are only applied as secondary references, Applicants do not address them separately at this time.

Applicants have earnestly tried to respond to each point raised by the Examiner in the official action. Applicants therefore respectfully request that the Examiner find all currently pending claims in condition for allowance.

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Respectfully submitted,

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Version With Markings to Show Changes Made

Claim 1 (Amended). An electronic package, comprising:

a conductive trace layer having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads;

a dielectric substrate mounted on the first side of the conductive trace layer;

a capacitor having a capacitance of from about 1 nF/sq.cm. to about 100 nF/sq.cm. including a first conductive layer, a second conductive layer and a layer of dielectric material disposed between the first and the second conductive layers, the first conductive layer mounted adjacent to the second side of the conductive trace layer;

a plurality of interconnect regions extending through the first conductive layer and the dielectric material layer of the capacitor; and

an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected to a first set of the interconnect pads and the second conductive layer of the capacitor being electrically connected to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

Claim 19 (Amended). The electronic package of claim 18 [1] wherein the dielectric substrate has an aperture extending therethrough adjacent to each solderball pad.